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10/788,899	02/27/2004	Kevin Torek	303.866US1	4587

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SCHWEGMAN, LUNDBERG & WOESSNER, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
ALANKO, ANITA KAREN	
ART UNIT	**PAPER NUMBER**
1792	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/788,899	TOREK ET AL.	
	Examiner	Art Unit	
	Anita K. Alanko	1792	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 8-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1 and 3* is/are allowed.

6)☒ Claim(s) *4-6 and 8-50* is/are rejected.

7)☐ Claim(s) *2* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2, 8, 9-21 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 2, the term "a polysilicon sacrificial second film" renders the metes and bounds of the claim unclear since it is unclear whether it refers to the same layer or a different layer from the second dielectric layer (claim 1, line 3). If it refers to the same layer, then the term lacks proper antecedent basis.

In claim 8, the terms "a dielectric first film" and "a sacrificial second film" render the metes and bounds of the claim unclear since it is unclear whether they refer to the same layer or different layers from the first and second dielectric layers (claim 1, lines 2-3). If they refer to the same layers as in the base claim, then the terms lack proper antecedent basis.

In claim 9, it appears that the terms "a dielectric first film" (line 5) and "a sacrificial second film" (line 6) lack proper antecedent basis. The term "sacrificial second film" is also used in claims 11-21.

Claims 10-21 are rejected because they fail to cure the indefiniteness of their base claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 46-50 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Lee et al (KR 2001-037699 A).

Lee discloses a process comprising:

forming a recess in a first dielectric stack including a first dielectric layer 110 (a nitride layer) on a substrate (layers 10-90) and a second dielectric layer 120 (an oxide layer) formed of a material different from the first dielectric layer (abstract, lines 11-13, the dry etch step);

forming a conductive structure 130 in the recess having vertical sidewalls (the figures depict vertical sidewalls), wherein the conductive structure is partially embedded in the recess and is formed to extend above the first dielectric stack (see Figure 2b where layer 130 is above 120 and thus extends above the first dielectric stack); and

electrically isolating the conductive structure (the etch-back step, abstract, line 15).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al (KR 2001-037699 A) in view of Choi (US 6,080,594) and O'Brien (US 5,817,182)

Lee discloses a process comprising:

forming a first dielectric layer 110 on a substrate (layers 10-90);

forming a second dielectric layer 120 on the first dielectric layer;

forming a first recess in the first and second dielectric layer to expose a portion of the substrate (abstract, lines 11-13, the dry etch step);

forming a conductive structure 130 in the first recess having vertical sidewalls (the figures depict vertical sidewalls);

first etching ("etch-back process" or SOG elimination, abstract, lines 15-16) to expose a first portion of the conductive structure;

second non-wet etching (dry etch, abstract, lines 16-18) to expose a second portion of the conductive structure.

Lee fails to disclose (in the abstract) how the etch-back is performed, or how the SOG is eliminated.

Choi teaches that SOG can be eliminated by using wet etching (col.8, lines 24-27). It would have been obvious to one with ordinary skill in the art to use a first wet etching process to expose a first portion of the conductive structure in the method of Lee because Choi teaches that this is a useful technique for eliminating SOG.

Lee fails to teach first rinsing of the conductive structure.

O'Brien teaches that it is useful to rinse after etching in order to remove etchant residues that may impact subsequent processing, device yield or reliability (col.4, lines 8-13). It would have been obvious to rinse after exposing the conductive structure in the modified method of Lee

because O'Brien teaches that it is useful to rinse after etching in order to remove etchant residues that may impact subsequent processing, device yield or reliability.

As to claim 4, Choi teaches that the first etching includes a wet process (SOG removal) and Lee discloses that the second etching is a dry process (dry etch).

As to claim 5, Lee teaches that the substrate includes a single dielectric stack 110,120, however the abstract does not disclose how they are deposited. It would have been obvious to one with ordinary skill in the art to form by vapor deposition since it is a conventional technique for forming dielectric layers.

Claims 6, 8-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al (KR 2001-037699 A) in view of Choi (US 6,080,594), O'Brien (US 5,817,182) and Kang et al (US 2004/0175884 A1).

The discussion of modified Lee from above is repeated here.

As to claim 6, Lee does not disclose the composition of an oxide. Kang teaches that a useful composition for forming capacitors similar to Lee is phospho silicate glass 220 ([0037]). It would have been obvious to one with ordinary skill in the art to form PSG as the oxide in the modified method of Lee because Kang teaches that it is a useful composition for forming oxides in methods to form capacitors.

As to claims 8-9, the modified method of Lee discloses to form the recess in a dielectric first and second film 110, 120 that is disposed above the substrate 10-90, and that oxide 120 of Lee is useful to form, as taught by Kang, to be PSG sacrificial second film 220 (since it is removed in Fig.3G). It would have been obvious to one with ordinary skill in the art that the

second film (PSG in the modified method of Lee) is a sacrificial film because Kang teaches that it is useful to form the final product without the oxide film.

As to claims 10-11, Lee discloses etching the a polysilicon sacrificial second film that is disposed over the substrate (the etch-back to expose the 4th oxide).

As to claim 12, Lee and Choi do not disclose the etch rates. However, the etch rate is result effective variable since a fast etch rate saves time whereas a slow etch rate provides for more control. It would have been obvious to one with ordinary skill in the art to etch at the cited rates in the modified method of Lee because the etch rate appears to reflect a result-effective variable which can be optimized. See MPEP 2144.05 IIB.

As to claims 11-21, also see the rejection of claim 5.

Claims 40-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al (KR 2001-037699 A) in view of Jost et al (US 5,966,611) and Sell (US 2004/0147074 A1).

The discussion of Lee from above is repeated here.

As to claim 40, Lee discloses a process comprising:

stripping a material (SOG) from a conductive structure 130 (polysilicon) embedded therein having vertical sidewalls (see figures), wherein the conductive structure is coupled to a substrate active area 100.

Lee fails to teach that the material that is stripped is amorphous carbon.

Jost teaches that a sacrificial film 54 over a conductive structure 50 (Fig.4) may comprise silicon oxide or amorphous carbon (col.3, lines 43-48). Jost also teaches that the amorphous carbon may be selectively etched from polysilicon (col.4, lines 61-62). It would have been

obvious to one with ordinary skill in the art to selectively etch amorphous carbon from the conductive structure in the method of Lee because Jost teaches that it is a useful, alternative material for silicon oxide in methods to form capacitors.

Lee fails to explicitly disclose the aspect ratio. The aspect ratio determines the density and properties of the final device device, in that a higher aspect ratio.

Sell teaches that trench capacitors typically have aspect ratios within the range cited ([0020]). It would have been obvious to vary the aspect ratio to that cited because Sell teaches that they are a useful, typical value for trench capacitors.

As to claim 41, Lee discloses that the conductive structure includes a container capacitor and Jost teaches that the amorphous carbon may be striped by an oxygen plasma (col.4, lines 61-63).

As to claims 42-45, it would have been obvious to include a TEOS-silicon oxide, BPSG, or polysilicon a broadly cited, since they are conventional films in semiconductor devices.

Claims 22-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al (US 6,764,947 B1) in view of O'Brien (US 5,817,182).

As to claim 22, Chan discloses a process comprising:

first etching a sacrificial second film 26 (Fig.3b-3c) to expose a first portion (the portion defined by the undercut) of a conductive structure 18, wherein first etching includes a first etch chemistry and wherein first etching includes a first etch rate; and

second etching an amorphous carbon first film 22 to expose a second portion of the conductive structure 18 (as shown in Fig.3b), wherein second etching includes a second etch chemistry.

Chan fails to explicitly disclose rinsing the conductive structure. Chan teaches that cleaning may be used, as is apparent to those having ordinary skill in the art (col.4, lines 47-57). O'Brien teaches that it is useful to rinse after etching in order to remove etchant residues that may impact subsequent processing, device yield or reliability (col.4, lines 8-13). It would have been obvious to rinse the conductive structure in the method of Chan because O'Brien teaches that it is useful to rinse after etching in order to remove etchant residues that may impact subsequent processing, device yield or reliability.

As to claims 22, 23 and 29, Chan also fails to disclose the relative etch rates of the first etch rate and second etch rate. However, the etch rate is result effective variable since a fast etch rate saves time whereas a slow etch rate provides for more control. It would have been obvious to one with ordinary skill in the art to etch at the cited rates in the modified method of Chan because the etch rate appears to reflect a result-effective variable which can be optimized. See MPEP 2144.05 IIB.

As to claims 24-28, 30-39, Chan discloses that the sacrificial second film is a silicon oxide that may be formed "in a variety of manners" such as vapor deposition (col.3, lines 17-20). Chan fails to disclose whether the silicon oxide is doped or undoped. O'Brien teaches some useful silicon oxides such as doped and undoped (BPSG, TEOS col.1, line 50), which are obvious to spin-on process or vapor deposit since they are conventional processing techniques in

the art. It is also conventional to dope polysilicon as desired to achieve the desired level of conductivity.

Allowable Subject Matter

Claims 1-3 are allowed over the prior art.

Claim 2 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Response to Amendment

The rejection of claims 1-3 are withdrawn in view of the claim amendment adding that first and second dielectric layers are removed by etching. Lee does not disclose or suggest to remove the dielectric layers.

The remaining claims are rejected over Lee and Chan.

Response to Arguments

Applicant's arguments filed 8/27/07 have been fully considered but they are not persuasive to the extent they still apply.

Applicant argues that Lee has four oxide and two nitride layers, whereas the present application has two oxide layers. In response, the claim has open "comprising" language and thus is open to more layers than are cited in the claim. Substrate is also a broad term and may comprise layers deposited on the substrate as constituting part of the substrate. The claim could

be amended by adding more limiting language such as contiguous or citing the material of the substrate and that the material is etched.

Examiner acknowledges that drawings are idealized, however they are depicted as vertical, contrary to the drawings in Kang which were not perpendicular, and therefore did not read on the claimed invention.

Applicant argues that Lee's dry and then wet etching teaches away. This is not persuasive because it is obvious to vary the type of etching. Dry and then wet may be preferred, but it is also obvious and known in the art to use dry etching instead of wet etching or vice versa.

Examiner acknowledges that Lee's structure is in contact with the fourth oxide layer. That is why the rejection of claim 1 is withdrawn. The other claims have not been similarly amended.

Applicant argues that there is no suggestion to have capacitor walls extending above the surrounding dielectric support. In response, this argument is not commensurate in scope with the rejected claims.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anita K. Alanko whose telephone number is 571-272-1458. The examiner can normally be reached on Mon-Fri until 3:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571-272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Anita K Alanko/
Primary Examiner
Art Unit 1792